AMENDMENTS

In the Claims

Please amend the claims as follows:

1. – 2. (Canceled)

3. (Currently Amended) The method of claim ~~21~~ 4, wherein the first component is configured to electrically communicate with a component external to the wafer stack.

4. (Currently Amended) A method for producing a die assembly comprising:

providing a wafer stack having a first wafer and a second wafer arranged in an overlying relationship with each other, a first portion of the first wafer supporting a first component, a second portion of the first wafer supporting a second component, the first component and the second component being located between the first wafer and the second wafer;

exposing the first portion and the second portion of the first wafer by removing a portion of the second wafer; and

dicing the first wafer between the first component and the second component to form a first die assembly and a second die assembly, the first die assembly including the first portion of the first wafer that extends outwardly beyond the periphery of a first portion of the second wafer, and the second die assembly including the second portion of the first wafer that extends outwardly beyond the periphery of a second portion of the second wafer such that neither the first component nor the second component is located between the first wafer and the second wafer;

~~The method of claim 21,~~ wherein the wafer stack includes a third wafer, the second wafer being arranged at least partially between the first wafer and the third wafer; and

wherein exposing a portion of the first wafer comprises:

exposing ~~a~~ the first portion and second portion of the first wafer by removing a portion of the third wafer and the portion of the second wafer.

5. (Currently Amended) The method of claim ~~21~~ 7, wherein exposing the first portion and second portion of the first wafer comprises:

dicing the second wafer to enable detachment of the portion of the second wafer from the wafer stack; and

removing the portion of the second wafer from the wafer stack.

6. (Currently Amended) The method of claim ~~21~~ 4, wherein dicing the first wafer between the first component and the second component comprises:

performing a through-cut of the wafer stack to at least partially detach the first die assembly from the wafer stack.

7. (Currently Amended) A method for producing a die assembly comprising:

providing a wafer stack having a first wafer and a second wafer arranged in an overlying relationship with each other, a first portion of the first wafer supporting a first component, a second portion of the first wafer supporting a second component, the first component and the second component being located between the first wafer and the second wafer;

exposing the first portion and the second portion of the first wafer by removing a portion of the second wafer; and

dicing the first wafer between the first component and the second component to form a first die assembly and a second die assembly, the first die assembly including the first portion of the first wafer that extends outwardly beyond the periphery of a first portion of the second wafer, and the second die assembly including the second portion of the first wafer that extends outwardly beyond the periphery of a second portion of the second wafer such that neither the first component nor the second component is located between the first wafer and the second wafer;

wherein the first component is configured to electrically communicate with a component external to the wafer stack;

~~The method of claim 3,~~ wherein the second wafer defines a recessed portion, the recessed portion being arranged in an overlying relationship with the first component, the recessed portion being configured to enable a partial through-cut of the second wafer in a vicinity of the recessed portion such that the first component is not damaged during formation of the partial through-cut; and

wherein exposing the first portion and the second portion of the first wafer comprises:

performing a partial through-cut of the second wafer in the vicinity of the recessed portion such that the first component is not damaged by the partial through-cut.

8. (Previously Presented) The method of claim 4, wherein exposing the first portion and the second portion of the first wafer comprises:

exposing a portion of the second wafer by removing a portion of the third wafer.

9. (Previously Presented) The method of claim 5, wherein dicing the second wafer comprises:

performing a first partial through-cut and a second partial through-cut of the wafer stack to at least partially detach of a portion of the second wafer from the wafer stack, the portion of the second wafer to be detached being arranged between the first partial through-cut and the second partial through-cut.

10. – 21. (Canceled)

22. (Previously Presented) The method of claim 4, wherein:

the third wafer supports a third component; and

after exposing the first portion and second portion of the first wafer, the third component is located beyond the periphery of the second wafer such that third component is not located between the first wafer and the second wafer.

23. (Previously Presented) The method of claim 22, wherein:

the third wafer also supports a fourth component; and

the portion of the third wafer that was removed to expose the first portion and second portion of the first wafer was located between the third component and the fourth component.